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#14
Response
F JONES
6-7-02

Attorney Docket No.: NECV 16.966

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Kazuyoshi UENO

Serial No.: 09/490,705

Filed: January 24, 2000

Title: **SEMICONDUCTOR DEVICE AND A METHOD FOR
FORMING A VIA HOLE IN A SEMICONDUCTOR DEVICE**

Examiner: T. Tran

Group Art Unit: 2811

Assistant Commissioner of Patents
Washington, DC 20231

RESPONSE TO OFFICE ACTION UNDER 37 C.F.R. 1.116

SIR:

In response to the Final Office Action mailed on March 7, 2002, the period for responding thereto expiring after June 7, 2002, please consider the following remarks:

REMARKS

Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Foote, et al., (U.S. Patent No. 6,114,235), in view of Wetzel, (U.S. Patent No. 6,143,646).

Applicant respectfully disagrees with the Examiner's ground for this rejection. In the rejection, the Examiner indicates that Foote et al. discloses an interconnect pattern 14, referring to Fig. 1e. However, element 14 in Fig. 1e is not an interconnect. Instead, it is an active region representing an area within a semiconductor device, such as a contact, gate, line, drain/source or the like to be electrically connected to other areas through a local interconnect, (column 3, lines 48-52).

Thus, the rejection of claim 1 under 35 U.S.C. §103(a) should be withdrawn.

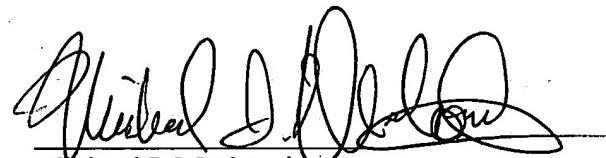
CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 1 is in condition for allowance. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

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Respectfully submitted,



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